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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/630,803 | 07/31/2003 | Shiro Sakiyama | 60188-601 | 9765 |

7590 01/10/2006

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| EXAMINER | |
|---|---|
| TAT, BINH C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/630,803 | SAKIYAMA ET AL. | |
| | Examiner | Art Unit | |
| | Binh C. Tat | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/630803 file on 06/19/02.

Claims 1-9 remain pending in the application.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Khouja et al. (US Patent 20040093531).

*3.* As to claim 1, Khouja et al. teach a cell library database composed of basic circuits of multiple types implementing various logics, the database containing: voltage value information which is given to at least one of a plurality of data terminals composed of input and output terminals included in the basic circuit and in which different voltage states of one node are represented in multiple bits (see fig 1-5 paragraph 0012-0020); and logical information between the input and output terminals including one or more said data terminals having the voltage value information (see fig 1-7 paragraph 0021-0031).

*4.* As to claim 2, Khouja et al. teach wherein the data terminal having the voltage value information represented in multiple bits is a power source terminal (see fig 1, fig 2 paragraph 0012-0018).

*5.* As to claim 3, Khouja et al. teach wherein the data terminal having the voltage value information represented in multiple bits is a digital input terminal or a digital output terminal (see fig 1, fig 2 paragraph 0012-0018).

*6.* As to claim 4, Khouja et al. teach wherein the data terminal having the voltage value information represented in multiple bits is an analog input terminal or an analog output terminal (see fig 1, fig 2 paragraph 0012-0018).

*7.* As to claim 5, Khouja et al. teach wherein the database further contains information on logic delays between the input and output terminals when logic changes occur therebetween (see fig 1-7 paragraph 0021-0031).

*8.* As to claim 6, Khouja et al. teach wherein the database further contains withstand voltage information for each of the basic circuits(see fig 1-7 paragraph 0021-0031).

*9.* As to claim 7, Khouja et al. teach a timing verification system for an integrated circuit composed of basic circuits of multiple types implementing various logics, the system comprising a cell library database which contains, for each of the basic circuits, voltage value information of a power source represented in multiple bits and given to at least one of a plurality of data terminals composed of input and output terminals included in the basic circuit (see fig 1, fig 2 paragraph 0012-0018), logical information between the input and output terminals including one or more said data terminals having the voltage value information of the power source (see fig 1, fig 2 paragraph 0012-0018), and information on logic delays between the input and output terminals when changes in the logical information occur therebetween (see fig 1-5 paragraph 0012-0020) wherein the system conducts timing verification by calculating a logic delay based on the information on logic delays according to the voltage value information from the data

terminal which has the voltage value information of the power source and is provided in each of the basic circuits constituting the cell library database (see fig 1-7 paragraph 0021-0031).

*10.* As to claim 8, Khouja et al. teach a withstand voltage verification system for an integrated circuit composed of basic circuits of multiple types implementing various logics, the system comprising a cell library database which contains (see fig 1, fig 2 paragraph 0012-0018), for each of the basic circuits (see fig 1-5 paragraph 0012-0020), voltage value information in which different voltage states of one node are represented in multiple bits and which is given to at least one of a plurality of data terminals composed of input and output terminals included in the basic circuit (see fig 1-5 paragraph 0012-0020), and withstand voltage information of the basic circuit, wherein the system conducts withstand voltage verification by comparing the voltage value information from the data terminal having the voltage value information with the withstand voltage information (see fig 1-7 paragraph 0021-0031).

*11.* As to claim 9, Khouja et al. teach wherein the data terminal having the voltage value information represented in multiple bits is a power source terminal (see fig 1-5 paragraph 0012-0020).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chaing can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
January 5, 2006

THUAN DO
Primary examiner.
1/07/06.